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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty. Dkt. No: 5310-03900

Inventor(s):
Thomas Skotnicki
Romain Gwoziecki

Title: SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND METHOD FOR MAKING SAME

CERTIFICATE OF EXPRESS MAIL
UNDER 37 C.F.R. §1.10

"Express Mail" mailing label number: EL893865074US
DATE OF DEPOSIT: December 11, 2001

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Washington, D.C. 20231

Derrick Brown

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

INTERNATIONAL APPLICATION NO.: PCT/FR00/01537
INTERNATIONAL FILING DATE: June 5, 2000
PRIORITY DATE CLAIMED: June 11, 1999
U.S. APPLICATION NO. (If known): Unknown

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. § 371.

2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. § 371.

3. ☐ This is an express request to begin national examination procedures (35 U.S.C. § 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. § 371(b) and PCT Articles 22 and 39(1).

4. ☒ A translation of the International Application into English (35 U.S.C. § 371(c)(2)), including a title page, 8 pages of specification, 3 pages of claims (claims 1-8), and a 1 page abstract.

5. ☒ Drawings
☒ Formal Figure(s) 1-3 on 2 sheet(s).

6. ☐ A copy of the International Application as filed (35 U.S.C. § 371(c)(2))
☐ is transmitted herewith including: _____ page abstract..
☐ has been transmitted by the International Bureau.
☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. § 371(c)(3))
   - ☒ are transmitted herewith (required only if not transmitted by the International Bureau).
   - ☐ have been transmitted by the International Bureau.
   - ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - ☐ have not been made and will not be made.
   - ☐ a translation of the amendments to the claims are transmitted here with.

8. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
   - ☐ A copy of the Demand for International Preliminary Examination is enclosed.

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. § 371(c)(4)):
   - ☐ is enclosed (_____ pages).
   - ☐ a combined Declaration and Power of Attorney is enclosed (_____ pages).
   - ☒ is not enclosed. Applicant requests the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail. Further, Applicant requests that the NOTICE OF MISSING PARTS-FILING DATE GRANTED be sent to the undersigned representative of Applicant.

10. ☒ Applicant hereby claims priority to:
    - ☒ International Application No.: PCT/FR00/01537 filed June 5, 2000.
    - ☒ French application No.: FR 99/07391 filed June 11, 1999.

11. ☐ A translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. § 371(c)(5)).

12. ☒ The entire disclosure of the International Application referred to above is considered to be part of the accompanying application and is hereby incorporated by reference herein.

13. ☐ Assignment Papers.
    - ☐ An assignment document is enclosed for recording (_____ pages).
    - ☐ Form PTO-1595 Assignment Recordation Cover Sheet (page).

14. ☒ A Preliminary Amendment (8 pages).

15. ☒ A substitute specification for pages 1-8, 12(9 pages).

16. ☒ A strikethrough version of specification and abstract (10 pages).

17. ☐ Power of Attorney
    - ☐ Is enclosed.
    - ☐ a combined Declaration and Power of Attorney is enclosed.

18. ☒ Information Disclosure Statement (IDS), including:
    - ☒ Form PTO-1449
    - ☒ Reference(s) marked according to Form PTO-1449.

19. ☒ Return Receipt Postcard

20. ☐ Small Entity Status
    - ☐ A small entity statement is enclosed.

21. ☐ Copy of PCT Form PCT/IB/338

22. ☐ Copy of International Request.

23. ☒ Copy of International Preliminary Examination Report.
☒ A copy of the International Preliminary Examination Report in French.
☐ English Translation of the International Preliminary Examination Report.

24. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR § 1.492 (a) (1)-(5): ☐ Neither international preliminary examination fee nor international search fee paid to USPTO and International Search Report not prepared by the EPO or JPO.....$970.00 ☒ International preliminary examination fee not paid to USPTO but International Search Report prepared by the EPO or JPO.....$890.00 ☐ International preliminary examination fee not paid to USPTO but international search fee paid to USPTO.....$760.00 ☐ International preliminary examination fee paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4).....$670.00 ☐ International preliminary examination fee paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4).....$96.00				
ENTER APPROPRIATE BASIC NATIONAL FEE AMOUNT (as selected above):				$890.00
Surcharge of $130.00 for furnishing oath or declaration later than ☐ 20 ☐ 30 Months from the earliest claimed priority date (37 C.F.R. § 1.492(e)).				
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	20 - 20 =	0	x $18.00 =	
Independent claims	3 - 3 =	0	x $78.00 =	
MULTIPLE DEPENDENT CLAIM(S)			+ $260.00 =	
TOTAL OF ABOVE CALCULATIONS:				$890.00
Reduction by 50% for Small Entity. A Small Entity Statement must be filed:				
SUBTOTAL:				$890.00
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Fee for recording the enclosed assignment. The assignment must be accompanied by an appropriate cover sheet. $40.00 per property:				
TOTAL FEES ENCLOSED:				$890.00

☒ A fee authorization in the amount of $890.00 is enclosed.

☐ Please charge my Deposit Account No. 50-1505/ in the amount of to cover the above fees.

☒ The Commissioner is hereby authorized to charge any other fees which may be required or credit any overpayment to Conley, Rose, & Tayon, P.C., Deposit Account No. 50-1505/5310-03900/EBM.

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Signature 

Name Mark R. DeLuca
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Date

PATENT 5310-03900

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: Unknown
Filed: Herewith
Inventor(s):
Thomas Skotnicki
Romain Gwoziecki

Title: SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND METHOD FOR MAKING SAME

Examiner: Unknown
Group/Art Unit: Unknown
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Derrick Brown

PRELIMINARY AMENDMENT

Commissioner for Patents
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Sir:

Please amend the above-captioned application as follows:

In the Specification:

Please replace pages 1-8 of the specification with pages 1-8 of the enclosed substitute sheets. Applicant has also submitted herewith a strikethrough version of the specification indicating the amendments.

In the Claims:

Please cancel claims 1-8 without prejudice.

Please add the following claims.

9. A semiconductor device, comprising:

a semiconductor substrate having a predetermined concentration, Ns, of a dopant of a first conductivity type;

a source region and a drain region doped with a dopant of a second conductivity type;

junctions, wherein the junctions delimit a channel region of a predetermined length, L_N, in the substrate, wherein the junctions are defined by the source region and the drain region;

first pockets located adjacent to each of the junctions, wherein the pockets have a predetermined length, Lp, wherein the first pockets are doped with a dopant of the first conductivity type with a dopant concentration, Np, which locally increases a net concentration in the substrate above Ns;

second pockets located adjacent to each of the junctions and stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, and wherein the second pockets are doped with a dopant of the second conductivity type with a dopant concentration, Nn, such that Nn is less than Np, which locally decreases a net concentration without changing a conductivity type, and wherein Nn is less than Ns; and

wherein an overall length of the first pockets and the second pockets is less than the length, L_N, of the channel region.

10. The semiconductor device of claim 9, wherein the second pockets comprise a plurality of elementary pockets stacked against each other.

11. The semiconductor device of claim 9, wherein the second pockets comprise a plurality of elementary pockets stacked against each other, wherein each elementary pocket comprises a rank, i, and a predetermined length, Ln_i, wherein a predetermined concentration, Nn_i, of a dopant of the second conductivity type satisfies the relationships:

$Ln_1 > Lp$;

$Ln_{i-1} < Ln_i < Ln_{i+1}$;

$Nn_{i-1} > Nn_i > Nn_{i+1}$; and

wherein the sum, ΣNn_i, of the concentrations of the dopant in the elementary pockets satisfies the relationship, $\Sigma Nn_i < Ns$.

12. The semiconductor device of claim 9, wherein the second pockets comprise a plurality of elementary pockets stacked against each other, and wherein the plurality of elementary pockets comprises three elementary pockets.

13. The semiconductor device of claim 9, wherein the semiconductor device comprises an MOS transistor.

14. The semiconductor device of claim 9, wherein the first conductivity type comprises p-type conductivity.

15. The semiconductor device of claim 9, wherein the second conductivity type comprises n-type conductivity.

16. A method for fabricating a semiconductor device, comprising:

forming a semiconductor substrate with a predetermined concentration, Ns, of a dopant of a first conductivity type;

forming a source region and a drain region by doping the source and drain regions with a dopant of a second conductivity type, wherein the second conductivity type is opposite the first conductivity type, wherein the source and drain regions form junctions that delimit a channel region between them, and wherein the channel region comprises a predetermined length, L_N;

forming first pockets adjacent to each of the junctions in the channel region, wherein the first pockets are formed by doping each of the first pockets with a predetermined concentration, Np, of a dopant of the first conductivity type, which locally increases a net concentration in the substrate above Ns, and wherein each of the first pockets comprises a predetermined length, Lp; and

implanting in the channel region a dopant of the second conductivity type under a set of conditions such that second pockets are formed in the channel region, wherein the second pockets are stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, wherein the second pockets have a concentration, Nn, of the dopant of the second conductivity type such that Nn is less than Np, which locally decreases a net concentration without changing a conductivity type, wherein Nn is less than Ns, and wherein the overall length of the first pockets and the second pockets is less than the nominal length, L_N, of the channel region.

17. The method of claim 16, wherein implanting in the channel region comprises a series of successive implanting steps such that the second pockets comprise a plurality of elementary pockets.

18. The method of claim 16, wherein implanting in the channel region comprises a series of successive implantion steps such that the second pockets comprise a plurality of elementary pockets, wherein each elementary pocket comprises a rank, i, and a predetermined length, Ln_i, and wherein a predetermined concentration, Nn_i, of a dopant of the second conductivity type satisfies the relationships:

$Ln_1 > Lp$;

$Ln_{i-1} < Ln_i < Ln_{i+1}$;

$Nn_{i-1} > Nn_i > Nn_{i+1}$; and

wherein the sum, ΣNn_i, of the concentrations of the dopant in the elementary pockets satisfies the relationship, $\Sigma Nn_i < Ns$.

19. The method of claim 18, further comprising increasing an implantation angle of incidence with respect to the normal angle to the substrate with each successive implantion step and decreasing an implantation dose with each successive implantion step.

20. The method of claim 18, wherein the successive implanting steps comprise implanting the dopant of the second conductivity type using a same angle of incidence with respect to the normal angle to the substrate, a same implantation dose, and a same implantation energy in each successive implantion step, the method further comprising annealing the device in an annealing step after each successive implantion step, wherein each annealing step is different.

21. The method of claim 16, wherein the set of conditions comprises an implantation angle of incidence with respect to the normal angle to the substrate, an implantation dose, and an implantation energy.

22. The method of claim 16, wherein the set of conditions comprises an implantation angle of incidence with respect to the normal angle to the substrate.

23. The method of claim 16, wherein the set of conditions comprises an implantation dose.

24. The method of claim 16, wherein the set of conditions comprises an implantation energy.

25. The method of claim 16, further comprising forming an MOS transistor with the semiconductor device.

26. The method of claim 16, wherein the first conductivity type comprises p-type conductivity.

27. The method of claim 16, wherein the second conductivity type comprises n-type conductivity.

28. A semiconductor device, comprising:

a semiconductor substrate having a concentration, Ns, of a dopant of a first conductivity type;

a source region and a drain region doped with a dopant of a second conductivity type;

junctions that define a channel region of a length, L_N, in the substrate, wherein the junctions are defined by the source region and the drain region;

first pockets located adjacent to each of the junctions, wherein the first pockets have a length, Lp, and wherein the first pockets are doped with a dopant of the first conductivity type with a dopant concentration, Np;

second pockets stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, wherein the second pockets are doped with a dopant of the second conductivity type with a dopant concentration, Nn, such that Nn is less than Np; and

wherein an overall length of the first pockets and the second pockets is less than the length, L_N, of the channel region.

In the Abstract:

Please replace the abstract with the enclosed substitute sheet. Applicant has also submitted herewith a strikethrough version of the abstract indicating the amendments.

It is believed that no fees are due in connection with the filing of this Preliminary Amendment. However, if any fees are due, the Assistant Commissioner is hereby authorized to deduct said fees from Conley, Rose & Tayon Deposit Account No. 50-1505/5310-03900/EBM.

Respectfully submitted,

Mark R. DeLuca
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Patent Agent for Applicant

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Date: 12/11/01

PATENT
5310-03900

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SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND METHOD FOR MAKING SAME

By:

Thomas Skotnicki

Romain Gwoziecki

Attorney Docket No.: 5310-03900

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SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND FABRICATION PROCESS

The present invention relates in general to a semiconductor device, such as an MOS transistor, in which there is compensation for the drop in the threshold voltage (V_{th}) due to the short channel effects, and to a process for fabrication such a semiconductor device.

For a given nominal channel length (L) of a transistor, the threshold voltage (V_{th}), in particular for short-channel transistors, that is to say those having a channel length of less than 0.25 μm and typically a channel length L of about 0.18 μm, drops suddenly.

The threshold voltage of a semiconductor device such as an MOS transistor, in particular a short-channel device, is a critical parameter of the device. This is because the leakage current of the device, for example, of the transistor, depends strongly on this threshold voltage. Taking into consideration the current supply voltages and those envisaged in the future (from 0.9 to 1.8 volts) for such devices and the permitted leakage currents (I_{off} of approximately 1 nA/μm), the threshold voltage V_{th} must have values of approximately 0.2 to 0.25 volts.

The sudden voltage drop (or roll-off) in the zones of the channel region of the semiconductor device results in dispersion of the electrical characteristics of the device and makes it difficult to obtain the desired threshold voltages.

To remedy this threshold voltage roll-off in semiconductor devices such as MOS transistors, it has been proposed, as described in the article "*Self-Aligned Control of Threshold Voltages in Sub-0 .2-μm MOSFETs*" by Hajima Kurata and Toshihiro Sugii, IEEE Transactions on Electron Devices, Vol. 45, No. 10, October 1998, to form, in the channel region, pockets adjacent to the source and drain region junctions and having a conductivity of the same type as the substrate, but the dopant concentration of which is greater than that of the substrate.

Although this solution reduces the threshold voltage roll-off gradient in the channel region, the short-channel effects lead to a more rapid roll-off of the threshold voltage V_{th} than the increase in the threshold voltage that can be obtained by incorporating the compensation pockets of the prior art.

Consequently, although these compensation pockets of the prior art allow partial local compensation for the roll-off of the threshold voltage V_{th}, it is thus not possible to obtain complete compensation for the roll-off over the entire channel region range desired.

The subject of the present invention is therefore a semiconductor device, such as an MOS transistor, which remedies the drawbacks of the devices of the prior art.

The subject of the present invention is more particularly a semiconductor device, such as an MOS transistor, whose voltage threshold roll-off due to the short-channel effects is almost fully compensated for, making it possible to achieve channel lengths which are arbitrarily small but non-zero.

The subject of the present invention is also a semiconductor device, such as an MOS transistor, having a constant threshold voltage V_{th} when the channel length L decreases down to very small effective channel lengths, for example 0.025 μm or less.

The subject of the present invention is also a process for fabricating a semiconductor device as defined above. This process may apply to devices having channels of arbitrarily small length, these being, moreover, technologically realizable.

The above objectives, according to the invention are achieved by fabricating a semiconductor device comprising a semiconductor substrate having a predetermined concentration Ns of a dopant of a first conductivity type, source and drain regions which are doped with a dopant of a second conductivity type, the opposite of the first, and define, in the substrate, junctions delimiting a channel region of predetermined nominal length L_N, and, in the channel region, a first pocket adjacent to each of the junctions and

having a predetermined length Lp, said first pockets being doped with a dopant of the first conductivity type but with a local concentration Np locally increasing the net concentration in the substrate, this device being characterized by the presence of at least one second pocket adjacent to each of the junctions and stacked against each of the first pockets, these second pockets having a length Ln such that $Ln > Lp$ and being doped with a dopant of the second conductivity type with a concentration Nn such that $Nn < Np$ locally decreasing the net concentration of the substrate but without changing the conductivity type.

According to a preferred embodiment of the invention, the second pockets comprise a plurality of elementary pockets stacked against one another, each elementary pocket of a given rank i having a predetermined length Ln_i and a predetermined concentration Nn_i of a dopant of the second conductivity type satisfying the following relationships:

$Ln_1 > Lp$

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} > Nn_i > Nn_{i+1}$, and

the sum ΣNn_i of the concentrations of the dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

In other words, the second pockets decrease the net concentration of dopant of the first conductivity type both in the first pockets and in the channel region, but do not change the conductivity type of the first pockets nor of the channel region.

The present invention also relates to a process for fabricating a semiconductor device as defined above which comprises the formation, in a semiconductor substrate having a predetermined concentration Ns of a dopant of a first conductivity type, of a source region and of a drain region which are doped with a dopant of a second conductivity type, the opposite of the first, the source and drain regions forming, in the substrate, junctions delimiting between them a channel region having a predetermined nominal length L_N, and the formation, in the channel region in a zone adjacent to each of the junctions, of a

first pocket having a predetermined length Lp and a predetermined concentration Np locally increasing the net concentration in the substrate above Ns, the process being characterized in that it furthermore comprises the implantation, in the channel region, of a dopant of the second conductivity type, the opposite of the first, under conditions such that at least one second pocket is formed in the channel region, this second pocket being stacked against each of the first pockets respectively, and having a length Ln such that Ln > Lp and a concentration Nn of a dopant of the first type such that Nn < Np and locally decreasing the net concentration in the substrate, but without changing the conductivity type.

In a preferred embodiment of the process of the invention, the implantation of the dopant of the second conductivity type consists of a series of successive implantations under conditions such that the second pockets formed each consist of a plurality of elementary pockets stacked against one another, each elementary pocket of a given rank i having a length Ln_i and a concentration Nn_i of a dopant of the second conductivity type satisfying the relationships:

$Ln_1 > Lp$

$Ln_{i-1} < Ln_i < Ln_{i+1}$

$Nn_{i-1} > Nn_i > Nn_{i+1}$ and

the sum ΣNn_i of the concentrations of the dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

The lengths Lp and Ln of the pockets are taken from the junctions.

Implantation of a dopant in a semiconductor substrate is a known process and it is possible, in the present process, to use any implantation process conventionally used in the technology of semiconductors.

As is known, the formation of doped pockets in a semiconductor substrate depends on the angle of incidence of the implantation with respect to the normal to the substrate, on the

implantation dose and on the implantation energy of the dopant. Thus, by varying the angle of incidence and the dopant dose, it is possible to increase the length of the implanted pocket and to vary the dopant concentration.

As a variant, in order to vary the length of the second implanted pockets and their dopant concentration, successive implantations may be carried out with the same angle of incidence with respect to the normal, the same dose and the same implantation energy but by subjecting the device after each successive implantation to an annealing heat treatment so as to make the dopant implanted in the substrate diffuse differently.

The remainder of the description refers to the appended figures, which show respectively:

- figure 1, a first embodiment of a semiconductor device, such as an MOS transistor, according to the invention;
- figure 2, a second embodiment of a semiconductor device according to the invention; and
- figure 3, a graph of the threshold voltage (V_{th}) for various semiconductor devices according to the invention as a function of the effective channel length.

Figure 1 shows a first embodiment of a semiconductor device according to the invention, such as an MOS transistor, comprising, as is conventional, a semiconductor substrate 1, for example a silicon substrate doped with a dopant of a first conductivity type, for example p-type conductivity, in which are formed source 2 and drain 3 regions doped with a dopant of a second conductivity type, the opposite of the first, for example an n-type dopant, which in the substrate define junctions 4, 5 delimiting between them a channel region 6.

As is known, the channel region 6 is covered with a gate oxide layer 11, for example a thin silicon oxide layer, which is itself surmounted by a gate 12, for example made of silicon. As is also well known, the gate 12 may be flanked on two opposed sides by spacers 13, 14 made of a suitable dielectric.

As is known, to reduce the rate of roll-off of the threshold voltage V_{th} in the channel region 6, two first pockets 7, 8 are formed in the channel region, each being adjacent to one of the junctions 4, 5 respectively. These pockets are doped by means of a dopant of the first conductivity type p, but with a concentration Np of dopant of the first type which locally increases the concentration in the substrate to above Ns and has a length Lp as short as possible.

According to the invention, two second pockets 9, 10 are formed in the channel region 6, which second pockets are each stacked against one of the first pockets, but with a length Ln greater than the length Lp of the first pockets, and are doped with a dopant of the second conductivity type, for example an n-type dopant, with a concentration Nn such that Nn is less than the concentration Np of dopant of the first conductivity type in the substrate.

Thus, in the zones of the second pockets, the net concentration of dopant of the first conductivity type, for example the p-type dopant, is decreased but the nature of the conductivity in the channel region is not changed, the channel still remaining a region of p-type conductivity.

Figure 2, in which the same reference numbers denote the same elements as previously, shows another embodiment of a semiconductor device according to the invention which differs from the previous device shown in figure 1 only by the fact that the second pockets 9, 10 consist in fact of pluralities of elementary pockets stacked against one another - three elementary pockets in the embodiment shown in figure 2.

Each elementary pocket of a given rank i has a length Ln_i and a concentration Nn_i of dopant of the second conductivity type which satisfy the following relationships:

$$Lp < Ln_i$$

$$Ln_{i-1} < Ln_i < Ln_{i+1}$$

$$Nn_{i-1} < Nn_i < Nn_{i+1}, \text{ and}$$

the sum ΣNn_i of the concentrations of dopant of the second conductivity type in the elementary pockets being such that:

$$\Sigma Nn_i < Ns.$$

In other words, the elementary pockets stacked against the first pockets 7 and 8 are also stacked against one another, but they have increasing lengths and, concurrently, concentrations of dopant of the first conductivity type which decrease as their lengths increase.

Moreover, the sum of the concentrations ΣNn_i of the stacked elementary pockets is such that it remains less than the concentration Ns of dopant of the first conductivity type in the substrate so that the conductivity type of the channel region 6 is not modified.

Thus, in the case shown in figure 2, in which the second pockets consist of three elementary pockets, the lengths and dopant concentrations of the elementary pockets satisfy the relationships:

$$Lp < Ln_1$$

$$Ln_1 < Ln_2 < Ln_3$$

$$Nn_1 > Nn_2 > Nn_3 \text{ and}$$

$$Nn_1 + Nn_2 + Nn_3 < Ns.$$

Figure 3 shows simulated graphs of the threshold voltage V_{th} for transistors having a gate oxide layer 4 nm in thickness and for a drain/source voltage of 1.5 volts as a function of the effective channel length. The lengths Lp and the concentrations Np of the first pockets doped with a dopant of the same type as the substrate correspond to the minimum channel length to be obtained and the highest doping.

Curve A corresponds to the stacking of a single second pocket according to the invention and shows that a flat V_{th} is obtained for a channel length down to 0.15 μm.

Curve B corresponds to the stacking of two second pockets according to the invention and shows that a flat V_{th} is obtained for a channel length down to 0.07 μm.

Finally, curve C corresponds to the stacking of seven second pockets according to the invention and shows that a flat V_{th} can be obtained for a channel length down to 0.025 μm.

Thus, the above curves show that the necessary doping levels remain reasonable and make it possible to obtain flat curves of V_{th} as a function of the effective channel length down to effective lengths of 25 nm, this being so even with gate oxide thicknesses of 4 nm.

CLAIMS AS AMENDED UNDER PCT ARTICLE 19

1. A semiconductor device comprising a semiconductor substrate (1) having a predetermined concentration Ns of a dopant of a first conductivity type, source (2) and drain (3) regions which are doped with a dopant of a second conductivity type; the opposite of the first, and define, in the substrate, junctions (4, 5) delimiting a channel region (6) of predetermined nominal length L_N and, in the channel region (6), a first pocket (7, 8) adjacent to each of the junctions (4, 5) and having a predetermined length Lp, said first pockets (7, 8) being doped with a dopant of the first conductivity type of concentration Np locally increasing the net concentration in the substrate above Ns, characterized in that it comprises, in the channel region (6), at least one second pocket (9, 10) adjacent to each of the junctions (4, 5) and stacked against each of the first pockets (7, 8), said second pockets (9, 10) having a length Ln such that Ln > Lp and being doped with a dopant of the second conductivity type with a concentration Nn such that Nn < Np and locally decreasing the net concentration of the substrate but without changing the conductivity type, and in that the concentration Nn of dopant of the second conductivity type in the second pockets satisfies the relationship Nn < Ns, the overall length of the first and second pockets being less than the nominal length L_N of the channel region.

2. The semiconductor device as claimed in claim 1, characterized in that the second pockets (9, 10) comprise a plurality of elementary pockets stacked against one another, each elementary pocket of a given rank i having a predetermined length Ln_i and a predetermined concentration Nn_i of a dopant of the second conductivity type satisfyingthe relationships:

$Ln_i > Lp$

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} > Nn_i > Nn_{i+1}$, and

the sum ΣNn_i of the concentrations of the dopant of the second conductivity type in the elementary pockets of the plurality satisfying the relationship $\Sigma Nn_i < Ns$.

3. The device as claimed in claim 1 or 2, characterized in that the device is an MOS transistor.

4. A process for fabricating a semiconductor device as claimed in claim 1 or 2, comprising:

- the formation, in a semiconductor substrate (1) having a predetermined concentration Ns of a dopant of the first conductivity type, of a source region (2) and of a drain region (3) which are doped with a dopant of a second conductivity type, the opposite of the first, said source and drain regions forming, in the substrate, junctions (4, 5) delimiting between them a channel region (6) having a predetermined nominal length L_N, and

- the formation, in the channel region (6) in a zone adjacent to each of the junctions (4, 5), of a first pocket (7, 8) having a predetermined length Lp and a predetermined concentration Np of a dopant of the first conductivity type locally increasing the net concentration in the substrate above Ns;

characterized in that it furthermore comprises:

- the implantation, in the channel region (6), of a dopant of the second conductivity type, the opposite of the first, under conditions such that at least one second pocket (9, 10) is formed in the channel region (6), this second pocket being stacked against each of the first pockets (7, 8) respectively, and having a length Ln such that $Ln > Lp$ and a concentration Nn of a dopant of the first type such that $Nn < Np$ and locally decreasing the net concentration in the substrate, but without changing the conductivity type, and in that concentration Nn of dopant of the second conductivity type in the second pockets satisfies the relationship $Nn < Ns$, the overall length of the first and second pockets being less than the nominal length L_N of the channel region.

5. The process as claimed in claim 4, characterized in that the implantation of the dopant of the second conductivity type consists of a series of successive implantations such that the second pockets (9, 10) each consist of a plurality of stacked elementary pockets, each elementary pocket of a given rank i having a length Ln_i and a concentration Nn_i of a dopant of the second conductivity type satisfying the relationships:

$Ln_1 > Lp$

$Ln_{i-1} < Ln_i < Ln_{i+1}$

$Nn_{i-1} > Nn_i > Nn_{i+1}$ and

the sum ΣNn_i of the concentrations of the dopant of the second conductivity type in the plurality of elementary pockets satisfying the relationship $\Sigma Nn_i < Ns$.

6. The process as claimed in claim 4 or 5, characterized in that the implantation conditions include the implantation angle of incidence with respect to the normal to the substrate, the implantation dose and the implantation energy.

7. The, process as claimed in claim 5, characterized in that, in the series of successive implantations, the angle of incidence with respect to the normal is increased and the implantation dose is decreased from one successive implantation to another.

8. The process as claimed in claim 5, characterized in that the series of successive implantations consists of implanting the dopant of the second conductivity type using the same angle of incidence with respect to the normal to the substrate, the same implantation dose and the same implantation energy, and, between each successive implantation, in subjecting the device to a different annealing treatment.

ABSTRACT

The invention concerns a semiconductor device comprising in the channel region (6) first voids (7,8) adjacent to the junctions (4, 5) which have a predetermined length Lp and a dopant concentration Np of a first conductivity type of the substrate (1) dopant locally increasing the net substrate concentration and second voids (9, 10) superposed on the first voids having a length Ln and a dopant concentration Nn of a second conductivity type opposed to the first conductivity type satisfying the relationships Ln > Lp and Nn < Np and locally decreasing the net substrate concentration but without modifying the type of conductivity. The invention is applicable to a MOS transistor.

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates in general to a semiconductor device, such as an MOS transistor, in which there is compensation for the drop in the threshold voltage (V_{th}) due to the short-channel effects, and to a process for fabrication of such a semiconductor device.

2. DESCRIPTION OF THE RELATED ART

For a given nominal channel length (L) of a transistor, the threshold voltage (V_{th})drops suddenly, in particular for short-channel transistors (i.e., those having a channel length of less than 0.25 μm and typically a channel length, L, of about 0.18 μm).

The threshold voltage of a semiconductor device such as an MOS transistor, in particular a short-channel device, is a critical parameter of the device. This is because the leakage current of the device (for example, of the transistor) depends strongly on the threshold voltage. Taking into consideration current supply voltages and those envisaged in the future (from 0.9 to 1.8 volts) for such devices and the permitted leakage currents (I_{off} of approximately 1 nA/μm), the threshold voltage V_{th} must have values of approximately 0.2 to 0.25 volts.

The sudden voltage drop (or roll-off) in the zones of the channel region of the semiconductor device results in dispersion of the electrical characteristics of the device and makes it difficult to obtain the desired threshold voltages.

To remedy this threshold voltage roll-off in semiconductor devices such as MOS transistors, it has been proposed, as described in the article "*Self-Aligned Control of Threshold Voltages in Sub-0 .2-μm MOSFETs*" by Hajima Kurata and Toshihiro Sugii,

IEEE Transactions on Electron Devices, Vol. 45, No. 10, October 1998, to form, in the channel region, pockets adjacent to the source and drain region junctions that have a conductivity of the same type as the substrate; but in which, the dopant concentration is greater than that of the substrate.

Although this solution reduces the threshold voltage roll-off gradient in the channel region, the short-channel effects lead to a more rapid roll-off of the threshold voltage, V_{th}, than the increase in the threshold voltage that can be obtained by incorporating the compensation pockets of the prior art.

Consequently, although these compensation pockets allow partial local compensation for the roll-off of the threshold voltage, V_{th}, it is not possible to obtain complete compensation for the roll-off over the entire channel region range desired.

Therefore a semiconductor device, such as an MOS transistor, that remedies the drawbacks of the devices of the prior art may be desired.

More particularly, a semiconductor device, such as an MOS transistor, whose voltage threshold roll-off due to the short-channel effects is almost fully compensated for may be desired. This makes it possible to achieve channel lengths which are arbitrarily small but non-zero.

Also a semiconductor device, such as an MOS transistor, may have a constant threshold voltage, V_{th}, when the channel length, L, decreases down to very small effective channel lengths, for example, 0.025 μm or less.

A process for fabricating a semiconductor device may apply to devices having channels of arbitrarily small length, these being, moreover, technologically realizable.

DESCRIPTION OF THE INVENTION

A semiconductor device is described that may have a semiconductor substrate with a predetermined concentration, Ns, of a dopant of a first conductivity type. The device may have source and drain regions which are doped with a dopant of a second conductivity type, which is opposite of the first conductivity type. Junctions delimiting a channel region of predetermined nominal length, L_N, may be defined in the substrate. A first pocket adjacent to each of the junctions and having a predetermined length, Lp, may be defined. The first pockets may be doped with a dopant of the first conductivity type but with a local concentration, Np, which locally increases the net concentration in the substrate. The device may include at least one second pocket located adjacent to each of the junctions and stacked against each of the first pockets. These second pockets may have a length, Ln, such that $Ln > Lp$. The second pockets may be doped with a dopant of the second conductivity type and have a concentration, Nn, such that $Nn < Np$. This may locally decrease the net concentration of the substrate without changing the conductivity type.

In an embodiment, the second pockets include a plurality of elementary pockets stacked against one another. Each elementary pocket of a given rank, i, may have a predetermined length, Ln_i, and a predetermined concentration, Nn_i, of a dopant of the second conductivity type satisfying the following relationships:

$Ln_1 > Lp$,

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} > Nn_i > Nn_{i+1}$, and

the sum, ΣNn_i, of the concentrations of the dopant of the second conductivity type in the elementary pockets may be such that:

$\Sigma Nn_i < Ns$.

In other words, the second pockets decrease the net concentration of dopant of the first conductivity type both in the first pockets and in the channel region. However, they do not change the conductivity type of the first pockets nor of the channel region.

A process for fabricating a semiconductor device as defined above is described. The process may include the formation of a source region and of a drain region in a semiconductor substrate having a predetermined concentration, Ns, of a dopant of a first conductivity type. The source region and the drain region may be doped with a dopant of a second conductivity type, which is opposite of the first conductivity type. The source and drain regions may form one or more junctions in the substrate such that the junctions delimit between them a channel region. The channel region may have a predetermined nominal length, L_N. In the channel region in a zone adjacent to each of the junctions, one or more first pockets may be formed having a predetermined length, Lp, and a predetermined concentration, Np. This may locally increase the net concentration in the substrate above Ns. The process may furthermore include the implantation, in the channel region, of a dopant of the second conductivity type, which is opposite of the first conductivity type. This may be done under a set of conditions such that at least one second pocket is formed in the channel region. Each second pocket may be stacked against each of the first pockets, respectively. The second pocket may have a length, Ln, such that $Ln > Lp$, and a concentration, Nn, of a dopant of the first type such that $Nn < Np$. This may locally decrease the net concentration in the substrate, without changing the conductivity type.

In a preferred embodiment, the implantation of the dopant of the second conductivity type consists of a series of successive implantations under a set of conditions such that the second pockets formed each consist of a plurality of elementary pockets stacked against one another. Each elementary pocket of a given rank, i, may have a length, Ln_i, and a concentration, Nn_i, of a dopant of the second conductivity type satisfying the relationships:

$Ln_1 > Lp$,

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} > Nn_i > Nn_{i+1}$, and

the sum, ΣNn_i, of the concentrations of the dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

The lengths Lp and Ln of the pockets are taken from the junctions.

Implantation of a dopant in a semiconductor substrate is a known process and it is possible, in the present process, to use any implantation process conventionally used in the technology of semiconductors.

As is known, the formation of doped pockets in a semiconductor substrate depends on the angle of incidence of the implantation with respect to the normal to the substrate, on the implantation dose, and on the implantation energy of the dopant. Thus, by varying the angle of incidence and the dopant dose, it is possible to increase the length of the implanted pocket and to vary the dopant concentration.

As a variant, in order to vary the length of the second implanted pockets and their dopant concentration, successive implantation steps may be carried out with the same angle of incidence with respect to the normal, the same dose, and the same implantation energy. However, subjecting the device to a different annealing heat treatment step after each successive implantation step may make the dopant implanted in the substrate diffuse differently for each implanted pocket.

BRIEF DESCRIPTION OF THE DRAWINGS

The remainder of the description refers to the appended figures, which show respectively:

Figure 1, a first embodiment of a semiconductor device, such as an MOS transistor;

Figure 2, a second embodiment of a semiconductor device; and

Figure 3, a graph of the threshold voltage (V_{th}) for various semiconductor devices as a function of the effective channel length.

DETAILED DESCRIPTION OF THE DRAWINGS

Figure 1 shows a first embodiment of a semiconductor device, such as an MOS transistor. The semiconductor device may include a semiconductor substrate 1, which may be, for example, a silicon substrate doped with a dopant of a first conductivity type (for example, p-type conductivity). Source 2 and drain 3 regions may be formed in the substrate 1 and doped with a dopant of a second conductivity type, which is opposite of the first conductivity type (for example, an n-type dopant). The source and drain regions may, in the substrate, define junctions 4, 5 delimiting between them a channel region 6.

The channel region 6 may be covered with a gate oxide layer 11 (for example, a thin silicon oxide layer), which is itself surmounted by a gate 12 (for example, a gate made of silicon). The gate 12 may be flanked on two opposed sides by spacers 13, 14 made of a suitable dielectric.

To reduce the rate of roll-off of the threshold voltage, V_{th}, in the channel region 6, two first pockets 7, 8 are formed in the channel region. Each pocket may be adjacent to one of the junctions 4, 5, respectively. These pockets are doped by means of a dopant of the first conductivity type, p, but with a concentration, Np, of dopant which locally increases the concentration in the substrate to above Ns and has a length, Lp, as short as possible.

Two second pockets 9, 10 are formed in the channel region 6. The second pockets are each stacked against one of the first pockets, but with a length, Ln, greater than the length, Lp, of the first pockets. The second pockets are doped with a dopant of the second conductivity type. For example, the dopant may be an n-type dopant with a concentration, Nn, such that Nn is less than the concentration Np of dopant of the first conductivity type in the substrate.

Thus, in the zones of the second pockets, the net concentration of dopant of the first conductivity type (for example, the p-type dopant) is decreased but the nature of the

conductivity in the channel region is not changed. The channel may still remain a region of p-type conductivity.

Figure 2, in which the same reference numbers denote the same elements as previously, shows another embodiment of a semiconductor device. Figure 2 shows that the second pockets 9, 10 may include pluralities of elementary pockets stacked against one another. For example, pluralities of elementary pockets may include three elementary pockets as shown in the embodiment in Figure 2.

Each elementary pocket of a given rank, i, has a length, Ln_i, and a concentration, Nni, of dopant of the second conductivity type which satisfy the following relationships:

$Lp < Ln_i$,

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} < Nn_i < Nn_{i+1}$, and

the sum ΣNn_i of the concentrations of dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

In other words, the elementary pockets stacked against the first pockets 7 and 8 are also stacked against one another. However, they have increasing lengths and, concurrently, concentrations of dopant of the first conductivity type which decrease as their lengths increase.

Moreover, the sum of the concentrations, ΣNn_i, of the stacked elementary pockets is such that it remains less than the concentration, Ns, of dopant of the first conductivity type in the substrate so that the conductivity type of the channel region 6 is not modified.

Thus, in the case shown in figure 2, in which the second pockets consist of three elementary pockets. The lengths and dopant concentrations of the elementary pockets satisfy the relationships:

$Lp < Ln_1$,

$Ln_1 < Ln_2 < Ln_3$,

$Nn_1 > Nn_2 > Nn_3$, and

$Nn_1 + Nn_2 + Nn_3 < Ns$.

Figure 3 shows simulated graphs of the threshold voltage, V_{th}, for transistors having a gate oxide layer 4 nm in thickness and for a drain/source voltage of 1.5 volts as a function of the effective channel length. The lengths, Lp, and the concentrations, Np, of the first pockets doped with a dopant of the same type as the substrate correspond to the minimum channel length to be obtained and the highest doping.

Curve A corresponds to the stacking of a single second pocket and shows that a flat V_{th} is obtained for a channel length down to 0.15 μm.

Curve B corresponds to the stacking of two second pockets and shows that a flat V_{th} is obtained for a channel length down to 0.07 μm.

Finally, curve C corresponds to the stacking of seven second pockets and shows that a flat V_{th} can be obtained for a channel length down to 0.025 μm.

Thus, the above curves show that the necessary doping levels remain reasonable and make it possible to obtain flat curves of V_{th} as a function of the effective channel length down to effective lengths of 25 nm. This may be so even with gate oxide thicknesses of 4 nm.

ABSTRACT

A semiconductor device may include a channel region formed between a source and a drain region. One or more first pockets may be formed in the channel region adjacent to junctions. The first pockets may be doped with a dopant of the first conductivity type. At least one second pocket may be formed adjacent to each of the junctions and stacked against each of the first pockets. The second pocket may be doped with a dopant of a second conductivity type such that the dopant concentration in the second pocket is less than the dopant concentration in the first pockets. The second pocket may reduce a local substrate concentration without changing the conductivity type of the channel region.

~~SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND FABRICATION PROCESS~~

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates in general to a semiconductor device, such as an MOS transistor, in which there is compensation for the drop in the threshold voltage (V_{th}) due to the short-channel effects, and to a process for fabrication of such a semiconductor device.

2. DESCRIPTION OF THE RELATED ART

For a given nominal channel length (L) of a transistor, the threshold voltage (V_{th})~~,~~ drops suddenly, in particular for short-channel transistors~~, that is to say~~ (i.e., those having a channel length of less than 0.25 μm and typically a channel length, L_g, of about 0.18 μm)~~, drops suddenly~~.

The threshold voltage of a semiconductor device such as an MOS transistor, in particular a short-channel device, is a critical parameter of the device. This is because the leakage current of the device~~,~~ (for example, of the transistor)~~,~~ depends strongly on ~~this~~ the threshold voltage. Taking into consideration ~~the~~ current supply voltages and those envisaged in the future (from 0.9 to 1.8 volts) for such devices and the permitted leakage currents (I_{off} of approximately 1 nA/μm), the threshold voltage V_{th} must have values of approximately 0.2 to 0.25 volts.

The sudden voltage drop (or roll-off) in the zones of the channel region of the semiconductor device results in dispersion of the electrical characteristics of the device and makes it difficult to obtain the desired threshold voltages.

To remedy this threshold voltage roll-off in semiconductor devices such as MOS transistors, it has been proposed, as described in the article "*Self-Aligned Control of Threshold Voltages in Sub-0 .2-μm MOSFETs*" by Hajima Kurata and Toshihiro Sugii, IEEE Transactions on Electron Devices, Vol. 45, No. 10, October 1998, to form, in the channel region, pockets adjacent to the source and drain region junctions ~~and~~ that have~~ing~~ a conductivity of the same type as the substrate~~;~~, but in which, the dopant concentration ~~of which~~ is greater than that of the substrate.

Although this solution reduces the threshold voltage roll-off gradient in the channel region, the short-channel effects lead to a more rapid roll-off of the threshold voltage, V_{th}, than the increase in the threshold voltage that can be obtained by incorporating the compensation pockets of the prior art.

Consequently, although these compensation pockets ~~of the prior art~~ allow partial local compensation for the roll-off of the threshold voltage, V_{th}, it is ~~thus~~ not possible to obtain complete compensation for the roll-off over the entire channel region range desired.

~~The subject of the present invention is t~~Therefore a semiconductor device, such as an MOS transistor, ~~which~~ that remedies the drawbacks of the devices of the prior ~~art~~art may be desired.

~~The subject of the present invention is m~~More particularly, a semiconductor device, such as an MOS transistor, whose voltage threshold roll-off due to the short-channel effects is almost fully compensated for may be desired.~~,~~ This make~~s~~ing it possible to achieve channel lengths which are arbitrarily small but non-zero.

~~The subject of the present invention is a~~Also a semiconductor device, such as an MOS transistor, may have~~ing~~ a constant threshold voltage, V_{th}, when the channel length, L, decreases down to very small effective channel lengths, for example, 0.025 μm or less.

~~The subject of the present invention is also a~~A process for fabricating a semiconductor device ~~as defined above. This process~~ may apply to devices having channels of arbitrarily small length, these being, moreover, technologically realizable.

DESCRIPTION OF THE INVENTION

~~The above objectives, according to the invention are achieved by fabricating a~~A semiconductor device is described that may have ~~comprising~~ a semiconductor substrate ~~having~~ with a predetermined concentration, Ns, of a dopant of a first conductivity type~~,~~. The device may have source and drain regions which are doped with a dopant of a second conductivity type, which is ~~the~~ opposite of the first conductivity type~~, and define, in the substrate,~~ jJunctions delimiting a channel region of predetermined nominal length, L_N, may be defined in the substrate~~, and, in the channel region,~~ aA first pocket adjacent to each of the junctions and having a predetermined length, Lp, may be defined. ~~said~~The first pockets may be~~ing~~ doped with a dopant of the first conductivity type but with a local concentration, Np, which locally increase~~sing~~ the net concentration in the substrate~~,~~. ~~this~~The device may ~~being characterized by the presence of~~include at least one second pocket located adjacent to each of the junctions and stacked against each of the first pockets~~,~~. ~~t~~These second pockets may have~~ing~~ a length, Ln, such that $Ln > Lp$. ~~and~~ The second pockets may be~~ing~~ doped with a dopant of the second conductivity type ~~with~~ and have a concentration, Nn, such that $Nn < Np$. This may locally decrease~~ing~~ the net concentration of the substrate ~~but~~ without changing the conductivity type.

~~According to a preferred~~In an embodiment ~~of the invention~~, the second pockets ~~comprise~~ include a plurality of elementary pockets stacked against one another~~,~~. ~~e~~Each elementary pocket of a given rank, i, may have~~ing~~ a predetermined length, Ln_i, and a predetermined concentration, Nn_i, of a dopant of the second conductivity type satisfying the following relationships:

$$Ln_1 > Lp,$$

$$Ln_{i-1} < Ln_i < Ln_{i+1},$$

$$Nn_{i-1} > Nn_i > Nn_{i+1}, \text{ and}$$

the sum, ΣNn_i, of the concentrations of the dopant of the second conductivity type in the elementary pockets may ~~be~~ing such that:

$$\Sigma Nn_i < Ns.$$

In other words, the second pockets decrease the net concentration of dopant of the first conductivity type both in the first pockets and in the channel region~~,~~. However, they ~~but~~ do not change the conductivity type of the first pockets nor of the channel region.

~~The present invention also relates to a~~A process for fabricating a semiconductor device as defined above is described. ~~which comprises~~ The process may include the formation of a source region and of a drain region~~,~~ in a semiconductor substrate having a predetermined concentration, Ns, of a dopant of a first conductivity type~~,~~. ~~of a~~ The source region and ~~of a~~the drain region ~~which are~~may be doped with a dopant of a second conductivity type, which is ~~the~~ opposite of the first conductivity type~~,~~. ~~t~~The source and drain regions ~~forming~~may form one or more junctions~~,~~ in the substrate~~,~~ such that the junctions delimit~~ing~~ between them a channel region. ~~having~~ The channel region may have a predetermined nominal length, L_N~~,~~. ~~and the formation, i~~In the channel region in a zone adjacent to each of the junctions, ~~of a~~ one or more first pockets may be formed having a predetermined length, Lp, and a predetermined concentration, Np. This may locally increase~~ing~~ the net concentration in the substrate above Ns~~,~~. ~~t~~The process ~~being characterized in that it~~may furthermore ~~comprises~~ include the implantation, in the channel region, of a dopant of the second conductivity type, which is~~the~~ opposite of the first conductivity type~~,~~. This may be done under a set of conditions such that at least one second pocket is formed in the channel region~~,~~. ~~this~~ Each second pocket may be~~ing~~ stacked against each of the first pockets, respectively~~,~~. The second pocket may ~~and~~ have~~ing~~ a length, Ln, such that Ln > Lp, and a concentration, Nn, of a dopant of the first type such that Nn < Np. This may~~and~~ locally decrease~~ing~~ the net concentration in the substrate, ~~but~~ without changing the conductivity type.

In a preferred embodiment ~~of the process of the invention~~, the implantation of the dopant of the second conductivity type consists of a series of successive implantations

under a set of conditions such that the second pockets formed each consist of a plurality of elementary pockets stacked against one another~~;~~. ~~e~~Each elementary pocket of a given rank, i, may have~~ing~~ a length, Ln_i, and a concentration, Nn_i, of a dopant of the second conductivity type satisfying the relationships:

$$Ln_1 > Lp,$$

$$Ln_{i-1} < Ln_i < Ln_{i+1},$$

$$Nn_{i-1} > Nn_i > Nn_{i+1}, \text{ and}$$

the sum, ΣNn_i, of the concentrations of the dopant of the second conductivity type in the elementary pockets being such that:

$$\Sigma Nn_i < Ns.$$

The lengths Lp and Ln of the pockets are taken from the junctions.

Implantation of a dopant in a semiconductor substrate is a known process and it is possible, in the present process, to use any implantation process conventionally used in the technology of semiconductors.

As is known, the formation of doped pockets in a semiconductor substrate depends on the angle of incidence of the implantation with respect to the normal to the substrate, on the implantation dose, and on the implantation energy of the dopant. Thus, by varying the angle of incidence and the dopant dose, it is possible to increase the length of the implanted pocket and to vary the dopant concentration.

As a variant, in order to vary the length of the second implanted pockets and their dopant concentration, successive implantations steps may be carried out with the same angle of incidence with respect to the normal, the same dose, and the same implantation energy~~.~~ ~~but by~~However, subjecting the device ~~after each successive implantation~~ to ~~an~~ a different annealing heat treatment step after each successive implantation step ~~so as to~~may make the dopant implanted in the substrate diffuse differently for each implanted pocket.

BRIEF DESCRIPTION OF THE DRAWINGS

The remainder of the description refers to the appended figures, which show respectively:

—fFigure 1, a first embodiment of a semiconductor device, such as an MOS transistor~~, according to the invention~~;

—fFigure 2, a second embodiment of a semiconductor device ~~according to the invention~~; and

—fFigure 3, a graph of the threshold voltage (V_{th}) for various semiconductor devices ~~according to the invention~~ as a function of the effective channel length.

DETAILED DESCRIPTION OF THE DRAWINGS

Figure 1 shows a first embodiment of a semiconductor device ~~according to the invention~~, such as an MOS transistor~~;~~. The semiconductor device may include~~comprising, as is conventional,~~ a semiconductor substrate 1, which may be, for example, a silicon substrate doped with a dopant of a first conductivity type~~,~~ (for example, p-type conductivity~~;~~). ~~in which are formed s~~Source 2 and drain 3 regions may be formed in the substrate 1 and doped with a dopant of a second conductivity type, which is~~the~~ opposite of the first conductivity type~~,~~ (for example, an n-type dopant~~;~~). ~~which~~ The source and drain regions may, in the substrate, define junctions 4, 5 delimiting between them a channel region 6.

~~As is known, t~~The channel region 6 ~~is~~ may be covered with a gate oxide layer 11~~,~~ (for example, a thin silicon oxide layer), which is itself surmounted by a gate 12~~,~~ (for example, a gate made of silicon). ~~As is also well known, t~~The gate 12 may be flanked on two opposed sides by spacers 13, 14 made of a suitable dielectric.

~~As is known, t~~To reduce the rate of roll-off of the threshold voltage, V_{th}, in the channel region 6, two first pockets 7, 8 are formed in the channel region~~;~~. ~~e~~Each pocket ~~being~~ may be adjacent to one of the junctions 4, 5, respectively. These pockets are doped

by means of a dopant of the first conductivity type, p, but with a concentration, Np, of dopant ~~of the first type~~ which locally increases the concentration in the substrate to above Ns and has a length, Lp, as short as possible.

~~According to the invention,~~ tTwo second pockets 9, 10 are formed in the channel region 6~~,~~. ~~which~~ The second pockets are each stacked against one of the first pockets, but with a length, Ln, greater than the length, Lp, of the first pockets~~,~~. ~~and~~ The second pockets are doped with a dopant of the second conductivity type~~,~~. ~~t~~For example, the dopant may be an n-type dopant~~,~~ with a concentration, Nn, such that Nn is less than the concentration Np of dopant of the first conductivity type in the substrate.

Thus, in the zones of the second pockets, the net concentration of dopant of the first conductivity type~~,~~ (for example, the p-type dopant~~,~~) is decreased but the nature of the conductivity in the channel region is not changed~~,~~. ~~t~~The channel may still remain~~ing~~ a region of p-type conductivity.

Figure 2, in which the same reference numbers denote the same elements as previously, shows another embodiment of a semiconductor device~~,~~ ~~according to the invention~~. Figure 2~~which differs from the previous device shown in figure 1~~shows ~~only by the fact~~ that the second pockets 9, 10 ~~consist in fact of~~may include pluralities of elementary pockets stacked against one another. ~~—~~For example, pluralities of elementary pockets may include three elementary pockets as shown in the embodiment ~~shown in figure~~ Figure 2.

Each elementary pocket of a given rank, i, has a length, Ln_i, and a ~~concentration Nn_i~~concentration, Nni, of dopant of the second conductivity type which satisfy the following relationships:

$$Lp < Ln_i,$$

$$Ln_{i-1} < Ln_i < Ln_{i+1},$$

$$Nn_{i-1} < Nn_i < Nn_{i+1}, \text{ and}$$

the sum ΣNn_i of the concentrations of dopant of the second conductivity type in the elementary pockets being such that:

$$\Sigma Nn_i < Ns.$$

In other words, the elementary pockets stacked against the first pockets 7 and 8 are also stacked against one another~~;~~ ~~but~~However, they have increasing lengths and, concurrently, concentrations of dopant of the first conductivity type which decrease as their lengths increase.

Moreover, the sum of the concentrations, ΣNn_i, of the stacked elementary pockets is such that it remains less than the concentration, Ns, of dopant of the first conductivity type in the substrate so that the conductivity type of the channel region 6 is not modified.

Thus, in the case shown in figure 2, in which the second pockets consist of three elementary pockets~~;~~ ~~t~~The lengths and dopant concentrations of the elementary pockets satisfy the relationships:

$$Lp < Ln_1,$$

$$Ln_1 < Ln_2 < Ln_3,$$

$$Nn_1 > Nn_2 > Nn_3, \text{ and}$$

$$Nn_1 + Nn_2 + Nn_3 < Ns.$$

Figure 3 shows simulated graphs of the threshold voltage, V_{th}, for transistors having a gate oxide layer 4 nm in thickness and for a drain/source voltage of 1.5 volts as a function of the effective channel length. The lengths, Lp, and the concentrations, Np, of the first pockets doped with a dopant of the same type as the substrate correspond to the minimum channel length to be obtained and the highest doping.

Curve A corresponds to the stacking of a single second pocket ~~according to the invention~~ and shows that a flat V_{th} is obtained for a channel length down to 0.15 μm.

Curve B corresponds to the stacking of two second pockets ~~according to the invention~~ and shows that a flat V_{th} is obtained for a channel length down to 0.07 μm.

Finally, curve C corresponds to the stacking of seven second pockets ~~according to the invention~~ and shows that a flat V_{th} can be obtained for a channel length down to 0.025 μm.

Thus, the above curves show that the necessary doping levels remain reasonable and make it possible to obtain flat curves of V_{th} as a function of the effective channel length down to effective lengths of 25 nm~~;~~. ~~t~~This may be~~ing~~ so even with gate oxide thicknesses of 4 nm.

ABSTRACT

~~The invention concerns a semiconductor device comprising in the channel region (6) first voids (7,8) adjacent to the junctions (4, 5) which have a predetermined length Lp and a dopant concentration Np of a first conductivity type of the substrate (1) dopant locally increasing the net substrate concentration and second voids (9, 10) superposed on the first voids having a length Ln and a dopant concentration Nn of a second conductivity type opposed to the first conductivity type satisfying the relationships Ln > Lp and Nn < Np and locally decreasing the net substrate concentration but without modifying the type of conductivity. The invention is applicable to a MOS transistor.~~

A semiconductor device may include a channel region formed between a source and a drain region. One or more first pockets may be formed in the channel region adjacent to junctions. The first pockets may be doped with a dopant of the first conductivity type. At least one second pocket may be formed adjacent to each of the junctions and stacked against each of the first pockets. The second pocket may be doped with a dopant of a second conductivity type such that the dopant concentration in the second pocket is less than the dopant concentration in the first pockets. The second pocket may reduce a local substrate concentration without changing the conductivity type of the channel region.

FIG.1

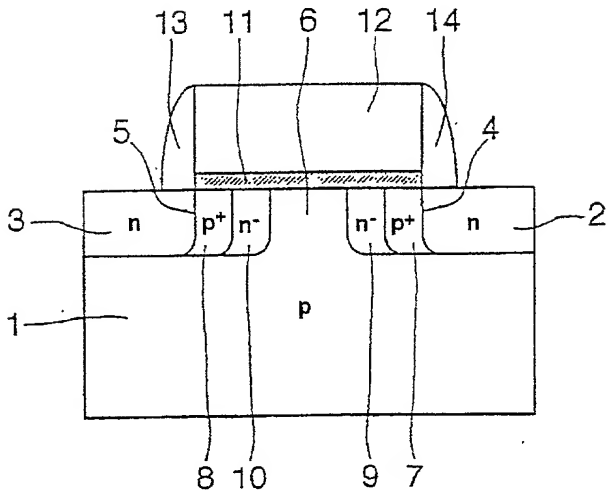

13
11
6
12
14
5
4
3
n
p+
n-
n-
p+
n
2
1
p
8
10
9
7

FIG.2

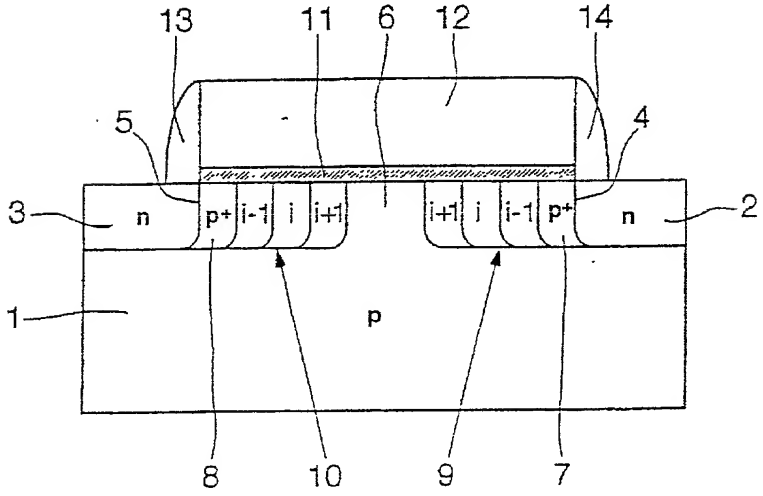
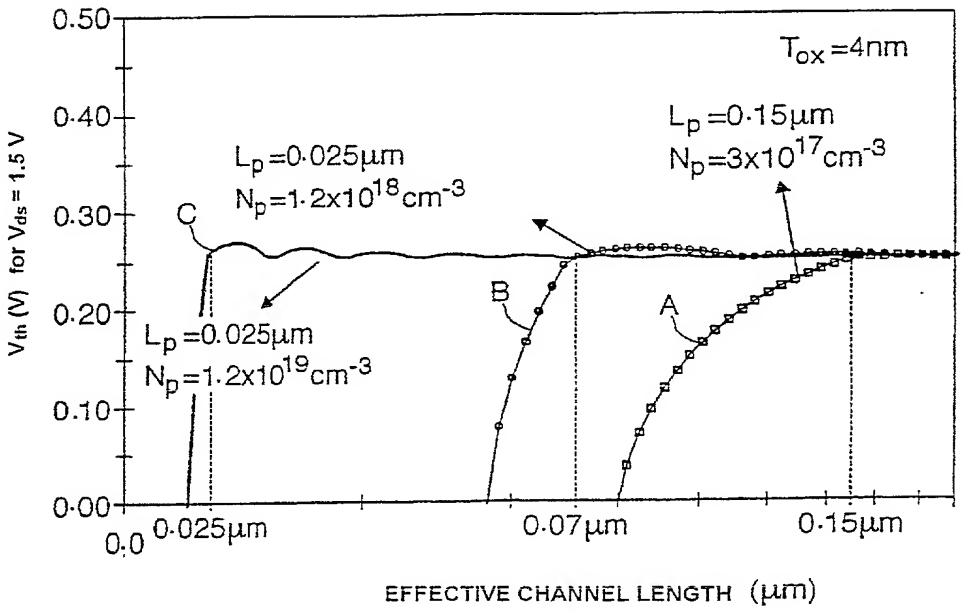

13
11
6
12
14
5
4
3
n
p+
i-1
i
i+1
i+1
i
i-1
p+
n
2
1
p
8
10
9
7

FIG.3


0.50
0.40
0.30
0.20
0.10
0.00
V_{th} (V) for V_{ds} = 1.5 V
T_{ox} =4nm
L_p =0·15μm
N_p=3x10^{17}cm^{-3}
L_p =0·025μm
N_p=1·2x10^{18}cm^{-3}
C
B
A
L_p =0.025μm
N_p=1·2x10^{19}cm^{-3}
0.0
0·025μm
0·07μm
0·15μm
EFFECTIVE CHANNEL LENGTH (μm)

DECLARATION AND POWER OF ATTORNEY
U.S.A.

Attorneys' Docket n°

As a below named inventor, I hereby declare that :

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original , first and sole inventor (if only one name is listed below), or the below named inventors believe they are the original, first and joint inventors (if plural names are listed below) , of the subject matter which is claimed and for which patent is sought on the invention entitled : SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND METHOD FOR MAKING SAME

whis is described and claimed in

(X) PCT International Application N° PCT/FR00/01537 filed June 5 2000
( ) the attached specification
AND (X) the specification in application Serial N°10/018,179Filed DECEMBER 11, 2001

and was amended on

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims , as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent Office all information known to me to be material to patentability of the subject matter claimed in this application , as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code , § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having filing date before that of the application on which priority is claimed :

Foreign/PCT Appln. N°	Country	Filing Date	Priority Claimed (Yes / No)
9907391	France	11 june 1999	Yes

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) or any PCT international application(s) designating the United States listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application or PCT International application in the manner provided by the first paragraph of Title 35, United States Code,§112, I acknowledge the duty to disclose information known to me to be material to the patentability of the subject matter claimed in this application ,as "materiality" is defined in Title 37, Code of Federal Regulations,§1.56 which become available between the filing date of the prior application and the national or PCT International filing date of this application :

U.S.Application N°	Filing Date	Status (patented/pending/abandoned)

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I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true ; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code; and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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